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EXAMINER	
MARTINEZ, DAVID E	
ART UNIT	**PAPER NUMBER**
2181	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,806	LAI ET AL.	
	Examiner	Art Unit	
	David E. Martinez	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22 and 24-29* is/are rejected.

7)☒ Claim(s) *5 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Fritz M. Fleming
FRITZ FLEMING
PRIMARY EXAMINER, Supervisory
GROUP 2100
AU 2181

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 5 and 23 are objected to because of the following informalities: Claims 5 and 23 recite subject matter disclosed in the specification (paragraphs 29-31), but not shown in the drawings, that being the third storage block. Figure 2 only shows a first and a second storage block (elements 58 and 60). Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5, 7, 15, 19 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regards to claims 5, lines 5-6, the term "blocking the controller from transferring data to the bus interface circuit" renders the claim indefinite. It is not understood if the controller is the element transferring data to a bus of if the applicant meant "blocking *the first storage block* from transferring data to the bus interface circuit if the second and third storage blocks are full". It was understood by the examiner that the controller only transfer data into the first and second storage blocks and not directly to the bus as disclosed by the applicant's specification (see applicant's abstract).

Claims 7, 15 and 27 contain the trademark/trade name "PCIX". Where a trademark or trade name is used in a claim as a limitation to identify or describe a particular material or product, the claim does not comply with the requirements of 35 U.S.C. 112, second paragraph. See *Ex parte Simpson*, 218 USPQ 1020 (Bd. App. 1982). The claim scope is uncertain since the trademark or trade name cannot be used properly to identify any particular material or

product. A trademark or trade name is used to identify a source of goods, and not the goods themselves. Thus, a trademark or trade name does not identify or describe the goods associated with the trademark or trade name. In the present case, the trademark/trade name is used to identify/describe a bus and, accordingly, the identification/description is indefinite.

With regards to claim 19, lines 4-6, the term "transferring a source data, whose size is greater than a storage capacity of the peripheral device, to the peripheral device;" renders the claim indefinite. It is not clear how a peripheral device having a fixed capacity is able to store source data whose size is greater than the size of the fixed capacity of the peripheral.

Due to the vagueness and a lack of clear definiteness used in the claims, the claims have been treated on their merits as best understood by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 6, 8-14, 16-22, 24-29 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication No. US 2002/0138697 A1 to Kanda.

1. With regards to claim 1, Kanda teaches a method of controlling data outputted [paragraph 39] from a peripheral device [figs 10, 11, 12, 13, 15, elements 107d, 107c, 107b, and 107a], the peripheral device being installed on a computer system [fig 1 is a computer system], the peripheral device comprising a bus interface circuit [fig 1, element 106 having figs 10, 11, 12, 13, 15, elements 202a-d] and a controller [fig 1 element 106 having fig 3 elements 402a-d inside element 202a-d inside element 106], the bus interface circuit being electrically connected

to a bus of the computer system [fig 3 line elements connecting element 106 to CPU I/F and DMA I/F] for controlling data transmission between the peripheral device and the bus, the controller being electrically connected to the bus interface circuit [fig 1 element 106 having fig 3 elements 402a-d inside element 202a-d inside element 106], the method comprising:

positioning at least a first storage block and a second storage block in the bus interface circuit [figs 10, 11, 12, 13, 15, elements 202a-d having pairs of toggle memory buffer elements 403];

storing data outputted from the controller in the first storage block [paragraphs 64, 65];

utilizing the bus interface circuit for simultaneously controlling the first storage block to transfer data stored in the first storage block to the bus and controlling the second storage block to store data outputted from the controller [paragraphs 64, 65. The buffers have to be bidirectional for the system to be able to retrieve data from the hard drives]; and

utilizing the bus interface circuit to control the second storage block to transfer data stored in the second storage block to the bus [paragraphs 64, 65].

2. With regards to claim 2, Kanda teaches the method of claim 1 further comprising:

while the second storage block outputs data to the bus, inputting data outputted from the controller into the first storage block [paragraph 65].

3. With regards to claim 3, Kanda teaches the method of claim 1 wherein a timing when the second storage block is full is prior to a timing when the first storage block completely outputs data stored in the first storage block [fig 12 shows a buffer 403 full prior to its pair buffer completely outputting data previously stored].

4. With regards to claim 4, Kanda teaches the method of claim 1 further comprising: before data stored in the first storage block are completely outputted to the bus, blocking the controller

from transferring data to the bus interface circuit if the second storage block is full [paragraph 65].

5. With regards to claim 6, Kanda teaches the method of claim 1 wherein a capacity of the first storage block is equal to a capacity of the second storage block [figs 10, 11, 12, 13, 15, elements 202a-d having pairs of toggle memory buffer elements 403, paragraphs 62-65].

6. With regards to claim 8, Kanda teaches the method of claim 1 wherein the peripheral device is a data-retrieving device [fig 1 elements 107a-d, also shown in figs 10, 11, 12, 13, 15].

7. With regards to claim 9, Kanda teaches the method of claim 8 wherein the data-retrieving device is a network card, a hard-disk drive, or an optical disk drive [fig 1 elements 107a-d, also shown in figs 10, 11, 12, 13, 15].

8. With regards to claim 10, Kanda teaches the method of claim 1 wherein the first and second storage blocks operate according to a first-in-first-out (FIFO) storage mechanism [fig 1, element 106 having figs 10, 11, 12, 13, 15, elements 202a-d having elements 402a-d having element 403 are shown to be FIFOS].

9. With regards to claim 11, Kanda teaches a computer system comprising:

a bus [fig 3 line elements connecting element 106 to CPU I/F and DMA I/F];

a peripheral device [figs 10, 11, 12, 13, 15, elements 107d, 107c, 107b, and 107a] comprising a bus interface circuit [fig 1, element 106 having figs 10, 11, 12, 13, 15, elements 202a-d] electrically connected to the bus, the bus interface circuit having at least a first storage block [] and a second storage block []; and

a controller [fig 1 element 106 having fig 3 elements 402a-d inside element 202a-d inside element 106] electrically connected to the bus interface circuit for simultaneously controlling the first storage block to transfer data stored in the first storage block to the bus and for controlling the second storage block to store data outputted from the controller [figs 10, 11,

12, 13, 15, elements 202a-d having pairs of toggle memory buffer elements 403, paragraphs 64, 65. The buffers have to be bidirectional for the system to be able to retrieve data from the hard drives].

10. With regards to claim 12, Kanda teaches the computer system of claim 11 wherein the bus interface circuit further comprises:

a first switch [fig 11, switch element between bus element 16 and buffer elements 43] electrically connected to the bus, the first storage block, and the second storage block for selectively connecting the bus with either the first storage block or the second storage block [paragraph 65]; and

a second switch electrically connected to the bus [fig 11, switch element between buffer elements 43 and elements 107a-d], the first storage block, and the second storage block for selectively connecting the controller with either the first storage block or the second storage block [paragraph 65].

11. With regards to claim 13, it's of the same scope as claim 3 above and thus is rejected under the same rationale.

12. With regards to claim 14, it's of the same scope as claim 6 above and thus is rejected under the same rationale.

13. With regards to claim 16, it's of the same scope as claim 8 above and thus is rejected under the same rationale.

14. With regards to claim 17, it's of the same scope as claim 9 above and thus is rejected under the same rationale.

15. With regards to claim 18, it's of the same scope as claim 10 above and thus is rejected under the same rationale.

16. With regards to claim 19, Kanda teaches a method of controlling data outputted from a peripheral device [figs 10, 11, 12, 13, 15, elements 107a-d], the peripheral device being installed on a computer system [fig 1 is a computer system], the method comprising:

transferring a source data, whose size is greater than a storage capacity of the peripheral device, to the peripheral device [paragraph 12]; and

while the peripheral device [figs 10, 11, 12, 13, 15, elements 107a-d] outputs the source data [data already stored in elements 107a-d] to a bus of the computer system [fig 3 line elements connecting element 106 to CPU I/F and DMA I/F], utilizing the peripheral device to receive the source data simultaneously [fig 11, peripheral interface elements 202a-d receive the data from elements 107a-d and output it to the system bus when reading from the hard drives. The buffers have to be bidirectional for the system to be able to retrieve data from the hard drives - paragraph 65];

wherein the peripheral device continuously occupies the bus until the source data are fully outputted to the bus [paragraphs 39, 65].

17. With regards to claim 20, Kanda teaches the method of claim 19 wherein the source data is inputted into a first storage block and a second storage block of the peripheral device [figs 10, 11, 12, 13, 15, elements 202a-d having pairs of toggle memory buffer elements 403, paragraphs 63-65].

18. With regards to claim 21, Kanda teaches the method of claim 20 wherein the source data is inputted into the first storage block first, and then the source data is inputted into the second storage block after the first storage block is full [figs 10, 11, 12, 13, 15, elements 202a-d having pairs of toggle memory buffer elements 403, paragraphs 63-65].

19. With regards to claim 22, Kanda teaches the method of claim 21 wherein when the source data is inputted into the second storage block, the source data stored in the first storage block is outputted to the bus simultaneously [paragraph 65].

20. With regards to claim 24, it's of the same scope as claim 3 above and thus is rejected under the same rationale.

21. With regards to claim 25, it's of the same scope as claim 4 above and thus is rejected under the same rationale.

22. With regards to claim 26, it's of the same scope as claim 6 above and thus is rejected under the same rationale.

23. With regards to claim 28, it's of the same scope as claim 8 above and thus is rejected under the same rationale.

24. With regards to claim 29, it's of the same scope as claim 9 above and thus is rejected under the same rationale.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7, 15 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication No. US 2002/0138697 A1 to Kanda in view of US Patent No. 6,529,989 to Bashford et al.(hereinafter Bashford)

25. With regards to claim 7, Kanda teaches the method is provided with the use of a hard drive expansion board connected to a bus in a personal computer [paragraphs 2-3], but he is

silent as to the method of claim 1 wherein the bus is a PCI bus or a PCIX bus, however, Bashford teaches a hard drive expansion board that uses the PCI standard for the benefit of using standards for increasing compatibility [fig 2, column 7-28].

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Kanda and Bashford to have the bus be a PCI bus for the benefit of using standards for increasing compatibility.

26. With regards to claim 15, it's of the same scope as claim 7 above and thus is rejected under the same rationale.

27. With regards to claim 27, it's of the same scope as claim 7 above and thus is rejected under the same rationale.

Allowable Subject Matter

Claim 5 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 5,521,928 to Worsley et al. teaches a triple ping pong buffer in fig 8 elements 900 and 901.

US Patent Application Publication No. US 20030079059 to Tsai teaches ping-pong/alternating buffers.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Martinez whose telephone number is (571) 272-4152. The examiner can normally be reached on 8:30-5:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DEM

Fritz M. Fleming
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3/6/2006